16 × 16 dot matrix units

LUM-2565MU304 / LUM-2565MU309

The LUM-2565MU series are 16 × 16 dot matrix displays which can be used in a wide range of applications, including alphabet, numeric, symbol and graphical displays. A large display can be easily created by arranging a number of these dot matrix displays in an array, and they can be applied to a variety of display purposes. A custom LSI controller has display data memory for two screens, and data for each screen can be written and displayed in turn.

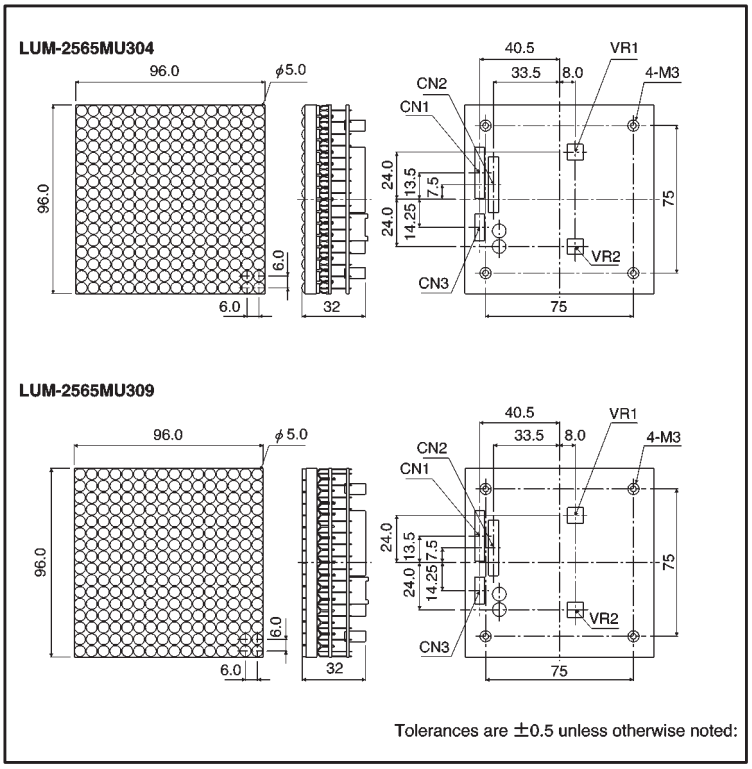
●Applications

Light source for displays

●Features

1) 16 × 16 dot matrix
   Circular emitters 5 mm in diameter.
2) Dimensions: 96 mm × 96 mm
3) Clear display.
4) Three-color display is possible (red, green, and orange).
5) 1/16 duty dynamic scan method.
6) Wide visibility angle (309 type).

●External dimensions (Units: mm)



●Selection guide

Display Type	Reflection Lamp	Cylinder Lamp
Type	LUM-2565MU304	LUM-2565MU309

LUM unit series

∗Omitting "LUM" from the part No.

		COB display type	Reflection LED type	High-luminance type	Chip LED type	Short louver chip LED type	Long louver chip LED type	Flat louver chip LED type
16 × 16 Dots	☐64 64×64mm		2563MU 302	2563ML 304				
	Dot size		ϕ3	ϕ3				
	Pin function		①	①				
	☐96 96×96mm			2565ML 304	2565HML 350			
	Dot size			ϕ5	☐ 2.1×2.3			
	Pin function			⑥	②			
16 × 32 Dots	☐40×2 40×80mm	5122MU 302			512CMU 300			
	Dot size	ϕ2			☐ 1.1×1.3			
	Pin function	⑦			⑨			
	☐ 64×2 64×128mm		5123MU 301		512HML300 / 512HML320		512HML 301	512HML 303
	Dot size		ϕ3		☐ 2.1×2.3		☐ 2.1×2.3	☐ 2.1×2.3
	Pin function		①		② / ⑩		②	②
	☐ 96×2 96×192mm		5125MU 302	512HY 350	512HML 350			
	Dot size		ϕ5	ϕ2	☐ 2.1×2.3			
	Pin function		⑧	⑪	②			
16 × 48 Dots	☐ 64×3 64×192mm				768HML 501			
	Dot size				☐ 2.1×2.3			
	Pin function				⑫			
24 × 24 Dots	☐ 96 96×96mm		5763MU 302	5763ML 302				
	Dot size		ϕ3	ϕ3				
	Pin function		③	③				
24 × 48 Dots	☐ 48×2 48×96mm	1151MU 301						
	Dot size	ϕ1.6						
	Pin function	⑤						
	☐ 96×2 96×192mm				115HML 300	115HML 301	115HML 302	115HML 303
	Dot size	ϕ1.6			☐ 2.1×2.3	☐2.1×2.3	☐ 2.1×2.3	☐2.1×2.3
	Pin function	⑤			④	④	④	④

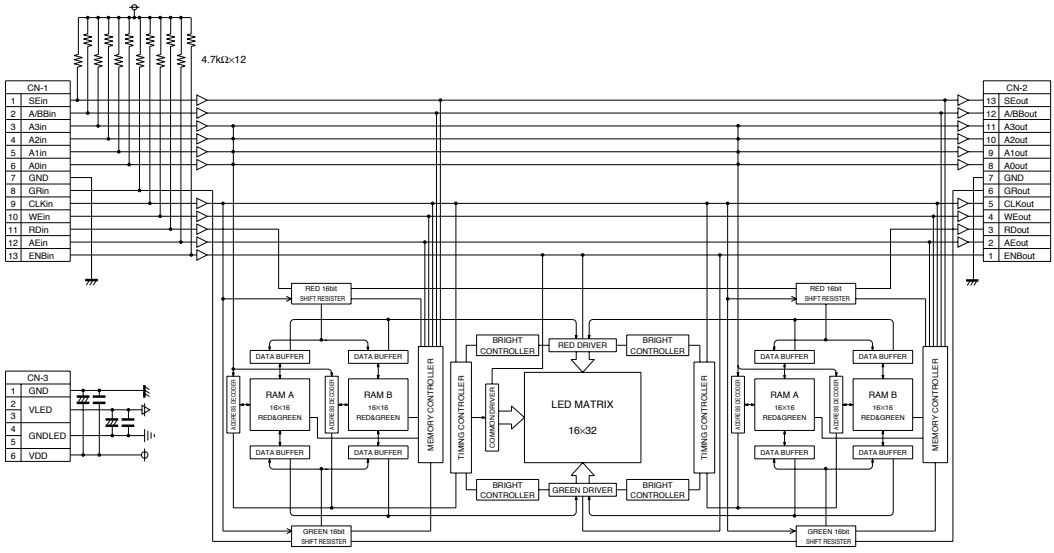
Note: Please refer to the page after regarding the pin function.

●Main specifications

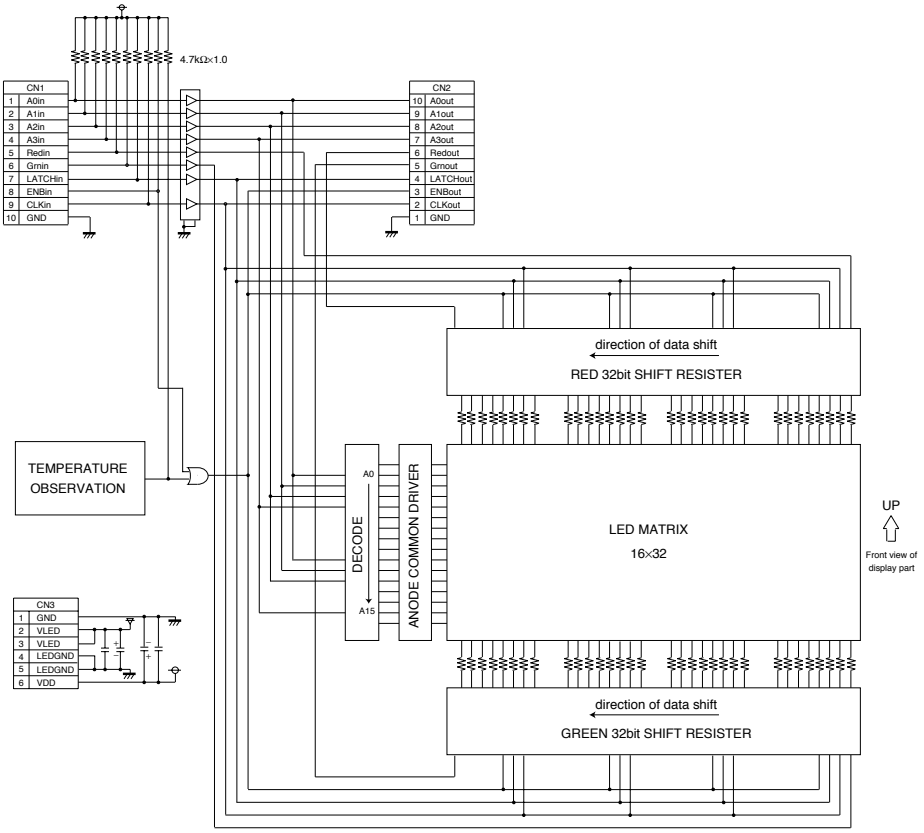
Size	Display Type	Type	Emitting color	Emitting material	Peak Wave-length (nm)	Dot Dia (mm)	Dot Pitch (mm)	Number of Dot (dot)	Control Circuit V_{DD} (V)	Control Circuit I_{CC1} Max. (mA)	Display Circuit V_{LED} (V)	Display Circuit I_{CC2} Max. (A)	Lumi-nance Typ. (cd / m²)	Opera-ting Frequ-ency Max. (MHz)	Driving System
□40 ×2	COB	LUM-5122MU302	Red	GaAsP	635	ϕ2	2.5	16 × 32	5	100	5	2.2	60	20	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								80		
	Chip LED	LUM-512CMU300	Ultra Red	AlGaInP	630	□ 1.1 × 1.3				80	4.5	2.0	100	13	
			Green	Gap	570								120		
□48 ×2	COB	LUM-1151MU301	Red	GaAsP	635	ϕ1.6	2	24 × 48	5	50	5	3.5	50	20	1 / 24 Duty Dynamic lighting up
			Green	Gap	563								100		
□64	Reflection Lamp Used Type Milky white	LUM-2563MU302	Red	GaAsP	635	ϕ3.0	4	16 × 16	5	50	5	2.8	100	20	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								100		
	Reflection Lamp Used Type Milky White	LUM-2563ML304	Ultra Red	GaAlAs	660								400		
			Green	Gap	563								300		
□64 ×2	Chip LED	LUM-512HML300	Ultra Red	GaAlAs	660	□ 2.1 × 2.3	4	16 × 32	5	30	5	2.7	130	20	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								130		
		LUM-512HML301	Ultra Red	GaAlAs	660								130		
			Green	Gap	563								130		
		LUM-512HML303	Ultra Red	GaAlAs	660								130		
			Green	Gap	563								130		
		LUM-512HML320	Ultra Red	GaAlAs	660					350		3.2	100	10	
			Green	Gap	563								100		
	Reflection Lamp Used Type Milky White	LUM-5123MU301	Red	GaAsP	635	ϕ3.0				100		5.6	100	20	
			Green	Gap	563								100		
□64 ×3	Chip LED	LUM-768HML501	Ultra Red	GaAlAs	660	□ 2.1 × 2.3	4	16 × 48	5	350	5	5.65	200	10	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								160		
□96	Reflection Lamp Used Type	LUM-2565ML304	Ultra Red	GaAlAs	660	ϕ5.0	6	16 × 16	5	20	5	5.5	600	20	1 / 8 Duty Dynamic lighting up
			Green	Gap	563								700		
	Chip LED	LUM-256HML350	Ultra Red	GaAlAs	660	□ 2.1 × 2.3	6	16 × 16	5	25	5	1.8	100	20	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								100		
□96 ×2	Reflection Lamp Used Type Milky white	LUM-5125MU302	Red	GaAsP	635	ϕ5.0	6	16 × 32	5	100	5	5.6	250	20	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								250		
	Chip LED	LUM-512HML350	Ultra Red	GaAlAs	660	□ 2.1 × 2.3	6	16 × 32	5	20	5	4.3	100	20	1 / 16 Duty Dynamic lighting up
			Green	Gap	563								100		
		LUM-512HY350	Yellow	AlGaInP	590	ϕ2.0				30		2.0	1200		
		LUM-115HML300	Ultra Red	GaAlAs	660	□ 2.1 × 2.3	4	24 × 48	5	50	5	4.0	100	20	1 / 24 Duty Dynamic lighting up
			Green	Gap	563								100		
		LUM-115HML301	Ultra Red	GaAlAs	660								100		
			Green	Gap	563								100		
		LUM-115HML302	Ultra Red	GaAlAs	660								100		
			Green	Gap	563								100		
		LUM-115HML303	Ultra Red	GaAlAs	660								100		
			Green	Gap	563								100		
□96	Reflection Lamp Used Type Milky white	LUM-5763MU302	Red	GaAsP	635	ϕ3.0	4	24 × 24	5	50	5	3.2	100	10	1 / 24 Duty Dynamic lighting up
			Green	Gap	563								100		
	Reflection Lamp Used Type Milky white	LUM-5763ML300	Ultra Red	GaAlAs	660								250		
			Green	Gap	563								250		

●Block diagrams

(1) Memory Type (LUM-512HML300 is advertised in here for just memory type of an example)



(2) Shift register type (LUM-512HML320 is advertised in here for just shift register type of an example)



●Pin descriptions

(1) CN-1

1) RDin

Data input for red LED. LED is on when this pin is HIGH, and off when it is LOW.

2) GRin

Data input for green LED. LED is on when this pin is HIGH, and off when it is LOW.

3) CLKin

Clock input. Used to load RDin and GRin data. Data is loaded into the internal shift registor at the leading edge of the CLK signal.

4) A0in - A3(A4)in

RAM address input. This specifies the address in memory to which display data will be written.

5) WEin

Write control signal. When this signal is HIGH, the contents of the internal shift registor are written to memory.
(Only valid when AEin is HIGH.)

6) AEin

Address control signal. When this signal is HIGH, the current address in A0in - A3(A4)in is specified.

7) A/ BBin

Control signal for selecting memory where data will be written. When this signal is HIGH, ARAM is selected, and when it is LOW, BRAM is selected. (Only valid when SEin is HIGH.) The contents of the memory not selected for writing will be displayed.

8) SEin

This signal determines whether memory selection will be made by external control or internal control. When this signal is HIGH, the A/ BBin signal determines whether ARAM or BRAM is selected. When ARAM is selected for writing, the BRAM data is displayed, and when BRAM is selected for writing, the ARAM data is displayed. When this signal is LOW, data will be written to a different memory (from address 0) after the last memory address (15 or 23) is written to. The display data will change simultaneously with the memory change.

9) ENBin

Display output is Enable. It becomes display state HIGH level, non-display state at Low level.

(2) CN-2

1) RDout

Data output for red LED. The signal is output simultaneously with CLK after passing through internal bit shift register 16 (24, 32, 48). If LED modules are connected serially, this pin will be connected to the next module's RDin pin.

2) GRout

Data output for green LED. The signal is output simultaneously with CLK after passing through internal bit shift register 16 (24, 32, 48). If LED modules are connected serially, this pin will be connected to the next module's RDin pin.

3) CLKout

Clock signal output. This pin outputs the CLKin signal. The pin connects to the next module's CLKin pin.

4) A0out - A3(A4)out

Address signal output. These pins output the signals of A0in - A3(A4)in. The pins connect to the next module's A0in - A3(A4)in pins.

5) WEout

WE (write control) signal output. This pin outputs the WEin signal. The pin connects to the next module's WEin pin.

6) AEout

AE (address control) signal output. This pin outputs the AEin signal. The pin connects to the next module's AEin pin.

7) A/BBout

A/BB (selection of memory for writing) signal output. This pin outputs the A/BBout signal. The pin connects to the next module's A/BBin pin.

8) SEout

SE (memory selection control) signal output. This pin outputs the SEin signal. The pin connects to the next module's SEin pin.

9) ENBout
ENB signal output. The ENBin signal is outputted. It is connected to ENBin of the next module.

●Shift register type pin function specifications

-CN1-

- CLKin Clock input. Used to load RDin and GRin data. Data is loaded into the internal shift registor at the leading edge of the CLK signal.
- Redin Data input for red LED. LED is on when this pin is HIGH, and off when it is LOW.
- Gmin Data input for green LED. LED is on when this pin is HIGH, and off when it is LOW.
- $\overline{\text{LATCHin}}$ Inputs a display data latch signal. The data is latched at Low and put through at High.
- $\overline{\text{ENBin}}$ Inputs a display enable signal. The display turns OFF at High and turns ON at Low.
- A0~A3in Inputs a common selection address signal. Specifies the common address in which the display data is output.

	A0	A1	A2	A3
ACOM0	0	0	0	0
ACOM1	1	0	0	0
ACOM2	0	1	0	0
ACOM3	1	1	0	0
ACOM4	0	0	1	0
ACOM5	1	0	1	0
ACOM6	0	1	1	0
ACOM7	1	1	1	0
ACOM8	0	0	0	1
ACOM9	1	0	0	1
ACOM10	0	1	0	1
ACOM11	1	1	0	1
ACOM12	0	0	1	1
ACOM13	1	0	1	1
ACOM14	0	1	1	1
ACOM15	1	1	1	1

- GND Control circuit ground.

-CN2-

- CLKout Clock signal output. This pin outputs the CLKin signal. The pin connects to the next module's CLKin pin.
- Redout Data output for red LED. The signal is output simultaneously with CLK after passing through internal bit shift register 16 (24, 32, 48). If LED modules are connected serially, this pin will be connected to the next module's RDin pin.
- Gmout Data output for green LED. The signal is output simultaneously with CLK after passing through internal bit shift register 16 (24, 32, 48). If LED modules are connected serially, this pin will be connected to the next module's GRin pin.
- $\overline{\text{LATCHout}}$ Outputs a display data latch signal. An LATCHin signal is output. Connect this to the next module's $\overline{\text{LATCHin}}$.
- $\overline{\text{ENBout}}$ Outputs a display enable signal. An $\overline{\text{ENBin}}$ signal is output. Connect this to the next module's $\overline{\text{ENBin}}$.
- A0~A3out Outputs a common selection address. An A0in-A3in signal is output. Connect this to the next module's A0in-A3in.
- GND Ground for the control circuit.

-CN3-

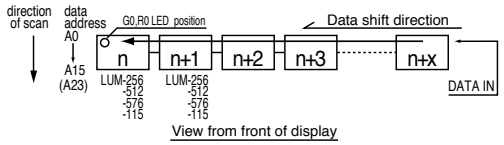
- •GND Control circuit & ground for the LED.
- •VLED Power supply for the LED.
- •VDD Power supply for the control circuit.

(3) CN-3

1) GND
   Control circuit ground.
2) VLED
   Supply voltage for LED.
3) GNDLED
   LED ground
4) VDD
   Supply voltage for control circuit.

●Attention points in handling LED dot matrix units

(1) Do not drop a dot matrix unit. This may cause deformation of the display or cracks in the solder.
(2) Be sure to mount the unit in the correct direction. Otherwise, the flow of data will be reversed.



(3) Excessive heat in the unit can cause a drop in luminosity and other operational problems. Use a fan or other means to ensure sufficient heat dissipation.
(4) The current required for the power supply varies greatly depending on the frequency of turning the LED on. Use a stable power supply which has sufficient capacity to handle sudden changes in load.
(5) When joining units together to form a panel, design the panel to allow sufficient overall heat dissipation and leave enough clearance for thermal expansion.
(As a general guideline, leave a gap of 0.3 mm between units.)
(6) Do not rub the display surface or use organic solvents such as thinner to clean the display surface.
(7) These units use high density LSI circuits. Therefore, take sufficient measures to protect them from electrostatic discharge.
(8) Do not short-circuit the units or apply unnecessarily high voltages to them.
(9) Do not use the units in conditions where the circuits will be directly exposed to wind and rain.
(10) If a unit is used at high frequency or if several units are connected together and the signal cable is long, noise may cause malfunctioning. In this case, use a shielded cable and terminate end components.
(11) As time passes, a difference in luminance may develop between LEDs which illuminate frequently and LEDs which do not. This will be particularly apparent if certain LEDs remain constantly illuminated.
(12) Ground the control circuit and LED close to the power supply equipment.

Note: This product may be classified as a strategic good (or function) determined by the foreign exchange and foreign trade laws. Therefore, when export this product, be sure to consult ROHM. This product is not designed for radiation resistance.

●**Pin functions** (LUM unit series diagram is correspondence to pin function)

(1)

No.	CN-1 signal name
1	SEin
2	A / BBin
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	GRin
9	CLKin
10	WEin
11	RDin
12	AEin

No.	CN-2 signal name
1	AEout
2	RDout
3	WEout
4	CLKout
5	GRout
6	GND
7	A0out
8	A1out
9	A2out
10	A3out
11	A / BBout
12	SEout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(2)

No.	CN-1signal name
1	SEin
2	A / BBin
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	GRin
9	CLKin
10	WEin
11	RDin
12	AEin
13	ENBin

No.	CN-2 signal name
1	ENBout
2	AEout
3	RDout
4	WEout
5	CLKout
6	GRout
7	GND
8	A0out
9	A1out
10	A2out
11	A3out
12	A / BBin
13	SEout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(3)

No.	CN-1 signal name
1	SEin
2	A / BBin
3	A4in
4	A3in
5	A2in
6	A1in
7	A0in
8	GND
9	GRin
10	CLKin
11	WEin
12	RDin
13	AEin

No.	CN-2 signal name
1	AEout
2	RDout
3	WEout
4	CLKout
5	GRout
6	GND
7	A0out
8	A1out
9	A2out
10	A3out
11	A4out
12	A / BBout
13	SEout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(4)

No.	CN-1 signal name
1	A / BBin
2	A4in
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	GRin
9	CLKin
10	WEin
11	RDin
12	AEin
13	ENBin

No.	CN-2 signal name
1	ENBout
2	AEout
3	RDout
4	WEout
5	CLKout
6	GRout
7	GND
8	A0out
9	A1out
10	A2out
11	A3out
12	A4out
13	A/ BBout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

LED displays

(5)

No.	CN-1 signal name
1	ENBin
2	AEin
3	RDin
4	WEin
5	CLKin
6	GRin
7	GND
8	A0in
9	A1in
10	A2in
11	A3in
12	A4in
13	A / BBin
14	SEin

No.	CN-2 signal name
1	ENBout
2	AEout
3	RDout
4	WEout
5	CLKout
6	GRout
7	GND
8	A0out
9	A1out
10	A2out
11	A3out
12	A4out
13	A / BBout
14	SEout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(6)

No.	CN-1 signal name
1	SEin
2	A / BBin
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	GRin
9	CLKin
10	WEin
11	RDin
12	AEin
13	ENBin
14	SDUTYin

No.	CN-2 signal name
1	SDUTYout
2	ENBout
3	AEout
4	RDout
5	WEout
6	CLKout
7	GRout
8	GND
9	A0out
10	A1out
11	A2out
12	A3out
13	A / BBout
14	SEout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(7)

No.	CN-1 signal name
1	SEin
2	A / BBin
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	GRin
9	CLKin
10	WEin
11	RDin
12	AEin
13	ENBin
14	OPEN

No.	CN-2 signal name
1	A / BBout
2	SEout
3	A2out
4	A3out
5	A0out
6	A1out
7	GRout
8	GND
9	WEout
10	CLKout
11	AEout
12	RDout
13	OPEN
14	ENBout

No.	CN-3 signal name
1	GND
2	VLED
3	GNDLED
4	VDD

(8)

No.	CN-1 signal name
1	SEin
2	A / BBin
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	GRin
9	CLKin
10	WEin
11	RDin
12	AEin
13	ENBin

No.	CN-2 signal name
1	AEout
2	RDout
3	WEout
4	CLKout
5	GRout
6	GND
7	A0out
8	A1out
9	A2out
10	A3out
11	A / BBout
12	SEout
13	ENBout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

LED displays

(9)

No.	CN-1 signal name
1	A0in
2	A1in
3	A2in
4	A3in
5	Redin
6	Grnin
7	$\overline{\text{LATCHin}}$
8	$\overline{\text{ENBin}}$
9	CLKin
10	GND

No.	CN-2 signal name
1	GND
2	CLKout
3	$\overline{\text{ENBout}}$
4	$\overline{\text{LATCHout}}$
5	Grnout
6	Redout
7	A3out
8	A2out
9	A1out
10	A0out

No.	CN-3 signal name
1	VLED
2	VLED
3	VCC
4	GND
5	GND

(10)

No.	CN-1 signal name
1	A0in
2	A1in
3	A2in
4	A3in
5	Redin
6	Grnin
7	$\overline{\text{LATCHin}}$
8	$\overline{\text{ENBin}}$
9	CLKin
10	GND

No.	CN-2 signal name
1	GND
2	CLKout
3	$\overline{\text{ENBout}}$
4	$\overline{\text{LATCHout}}$
5	Grnout
6	Redout
7	A3out
8	A2out
9	A1out
10	A0out

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(11)

No.	CN-1 signal name
1	SEin
2	A / BBin
3	A3in
4	A2in
5	A1in
6	A0in
7	GND
8	DATAin
9	CLKin
10	WEin
11	OPEN
12	AEin
13	ENBin

No.	CN-2signal name
1	ENBout
2	AEout
3	OPEN
4	WEout
5	CLKout
6	DATAout
7	GND
8	A0out
9	A1out
10	A2out
11	A3out
12	A / BBout
13	SEout

No.	CN-3 signal name
1	GND
2	VLED
3	VLED
4	GNDLED
5	GNDLED
6	VDD

(12)

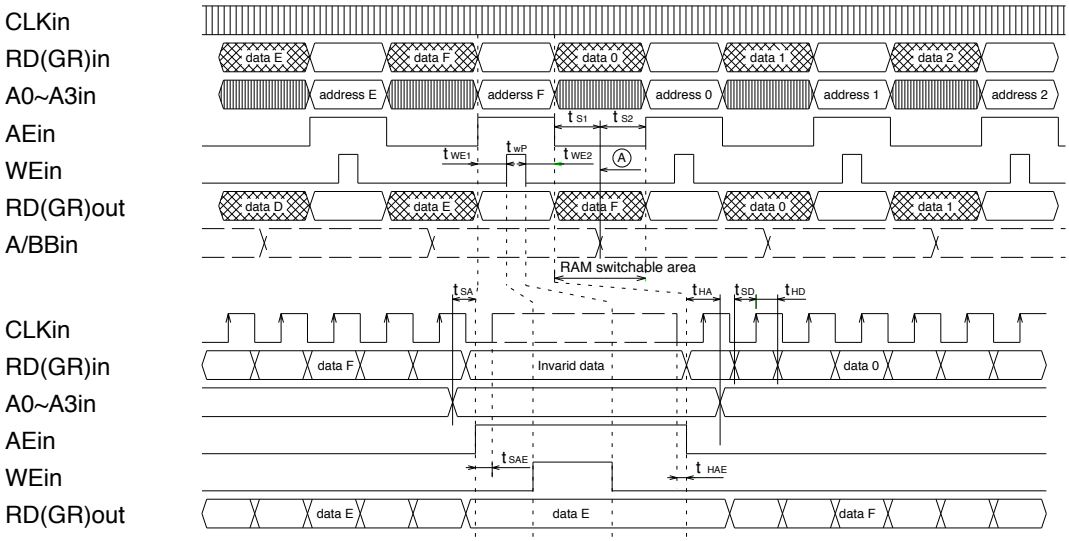
No.	CN-1 signal name
1	LEDCLKin
2	GND
3	LEDRin
4	LEDGin
5	LEDLATCHin
6	LEDENBin
7	LEDA3in
8	LEDA2in
9	LEDA1in
10	LEDA0in
11	GND
12	DC5V

No.	CN-2 signal name
1	LEDCLKout
2	GND
3	LEDRout
4	LEDGout
5	LEDLATCHout
6	LEDENBout
7	LEDA3out
8	LEDA2out
9	LEDA1out
10	LEDA0out
11	GND
12	DC5V

No.	CN-3 signal name
1	LEDGND
2	LEDGND
3	LEDGND
4	LEDGND
5	LEDDC5V
6	LEDDC5V
7	LEDDC5V
8	LEDDC5V

●Timing diagram

(1) 16×16, 16×32 Memory type



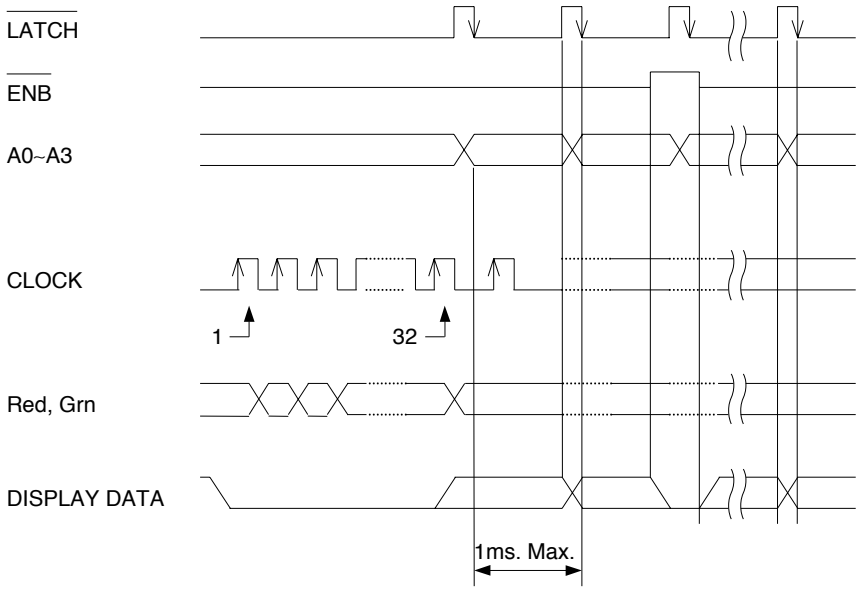
The display data are fetched at the leading edge of the clock and are outputted at the following adge.
Data are not fetched when AEin is "H", and the previous data are kept outputted on the display.
The RAM is switched by A/BB (SEin = "H") or when the address F A0~A3 is hold and AEin gose down.
When RAM is switched by A/BB, it is done by Ⓐ timing usually.
RAM switching timing changed over irrespective of display.
AEin is outputted while CLKin is "L".

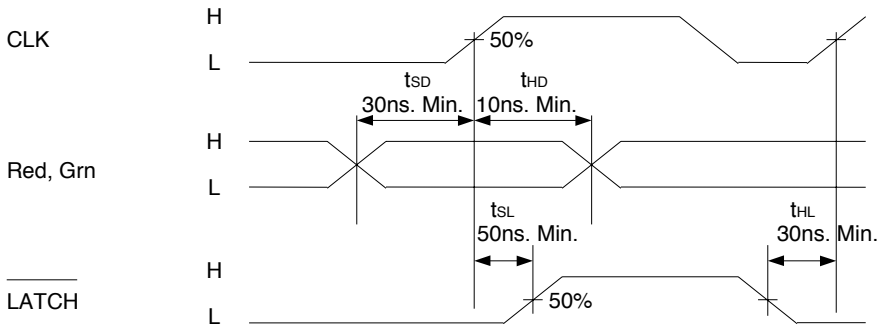
Parameter	Symbol	Min.	Typ.	Max.	Parameter	Symbol	Min.	Typ.	Max.
Clock frequency	f	–	–	20MHz	Address set-up time	t_{SA}	15	–	–
Address enable holding time (1)	t_{WE1}	10	–	–	Address hold time	t_{HA}	15	–	–
Address enable holding time (2)	t_{WE2}	10	–	–	Data set-up time	t_{SD}	10	–	–
Write pulse time	t_{WP}	30	–	–	Data hold time	t_{HD}	10	–	–
RAM selection time (1)	t_{S1}	15	–	–	Address enable set-up time	t_{SAE}	10	–	–
RAM selection time (2)	t_{S2}	15	–	–	Address enable hold time	t_{HAE}	5	–	–

(No indication units ns)

Controller unit input timing chart

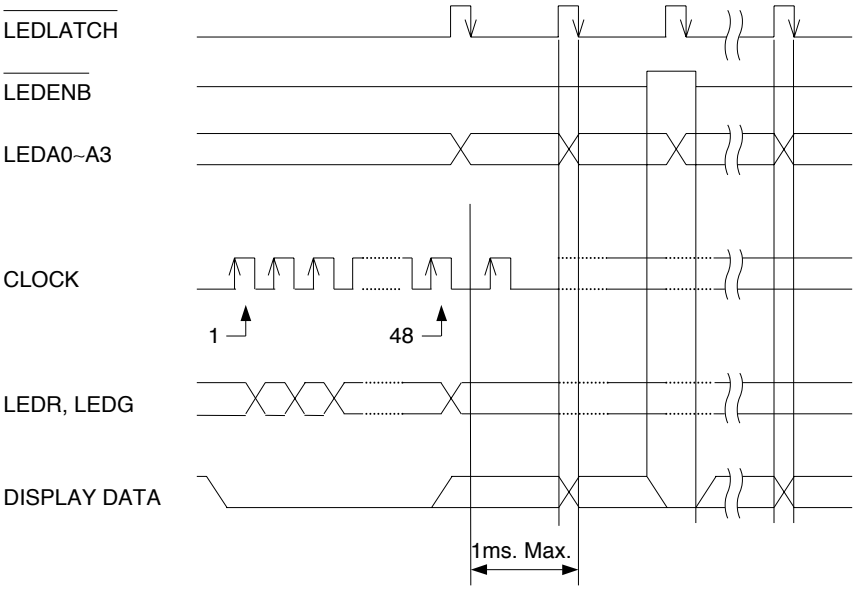
(2) 16×32 shift register type

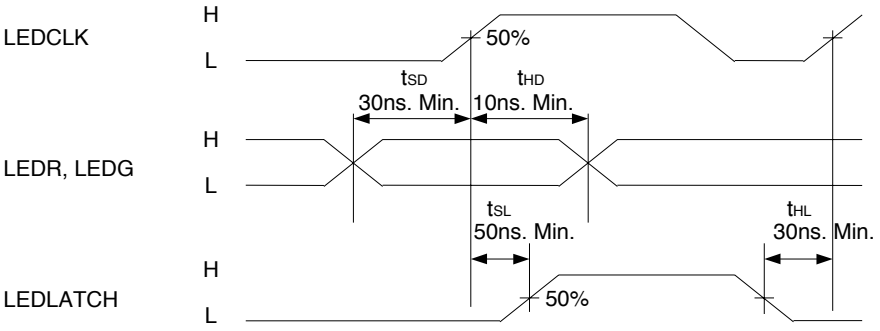




∗ If the value in the shift register changes while the LATCH signal status is "H", the latch data changes accordingly.

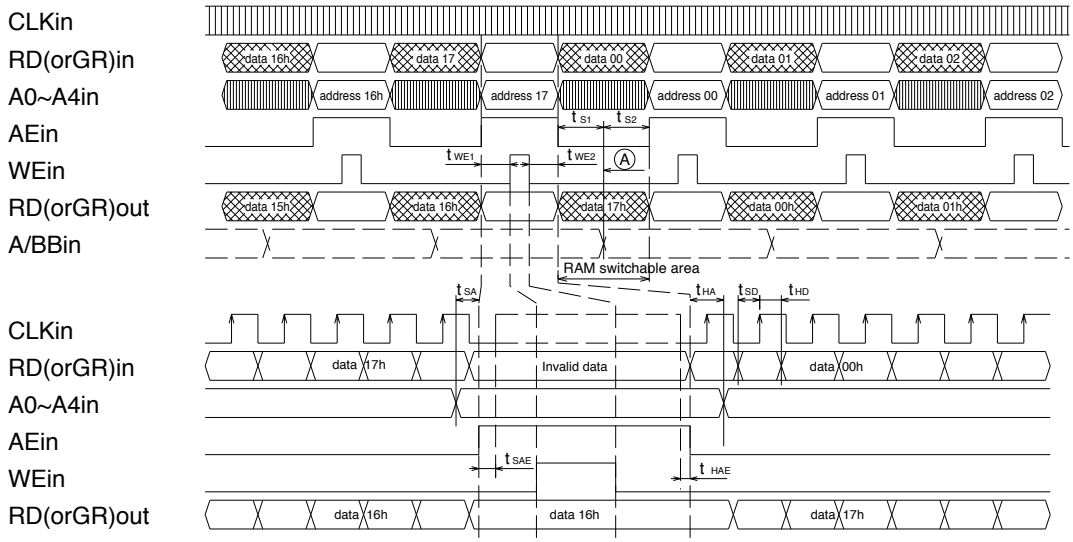
(3) 16×48 shift register type





∗ If the value in the shift register changes while the LATCH signal status is "H" the latch data changes accordingly.

(4) 24×24, 48×48 Memory type



The display data are fetched at the leading edge of the clock and are outputted at the following edge.
Data are not fetched when AEin is "H", and the previous data are kept outputted on the display.
Display data invalid when AE High.
The RAM is switched by A/BB (SEin = "H") or when the address A0~A4 is held at 17h and AEin is dropped.
RAM switching timing changed over irrespective of display.
When RAM is switched by A/BB, it is done by Ⓐ timing usually.
AEin is outputted while CLKin is "L".
If AE is dropped during CLK is "H", shift register data are shifted one bit.

Parameter	Symbol	Min.	Typ.	Max.	Parameter	Symbol	Min.	Typ.	Max.
Clock frequency	f	–	–	∗20MHz	Address set-up time	t_{SA}	0	–	–
Address enable holding time (1)	t_{WE1}	26	–	–	Address hold time	t_{HA}	10	–	–
Address enable holding time (2)	t_{WE2}	20	–	–	Data set-up time	t_{SD}	10	–	–
Write pulse time	t_{WP}	50	–	–	Data hold time	t_{HD}	10	–	–
RAM selection time (1)	t_{S1}	15	–	–	Address enable set-up time	t_{SAE}	10	–	–
RAM selection time (2)	t_{S2}	15	–	–	Address enable hold time	t_{HAE}	0	–	–

∗ Individual use (No indication units ns)

Controller unit input timing chart (24×24dots)